WHAT IS CLAIMED IS:

1. A semiconductor device comprising:

a gate electrode;

a gate insulator film wider than said gate electrode;

an active layer;

a pair of n- or p-type doped regions formed in said active layer;

a pair of silicide layers self-aligned to said gate insulator film, said silicide layers consisting mainly of a metal material and silicon;

a first metallization layer in intimate contact with said silicide layers, said first metallization layer being made of said metal material; and

a top layer of interconnect metal formed over said gate electrode and connected with said first metallization layer via at least one contact.

2. A device according to claim 1, wherein conductive interconnects and said gate electrode are formed in a common layer, and wherein said conductive interconnects are connected with said first metallization layer via at least one contact.

3. A device according to claim 1, further comprising a second metallization layer that is in intimate contact with said first metallization layer, similar in geometry to said first metallization layer, and made of a material having a smaller resistivity than the material of said first metallization layer.

4. A device according to claim 1, wherein said first

metallization layer consists mainly of an element selected from the group consisting of titanium, molybdenum, tungsten, platinum, chromium, and cobalt.

5. A semiconductor device comprising:

a gate electrode formed in a layer;

a gate insulator film wider than said gate electrode;

an active layer;

a pair of n- or p-type doped regions formed in said active layer;

a pair of silicide layers self-aligned to said gate insulator film, said silicide layers consisting mainly of a metal material and silicon;

a first metallization layer in intimate contact with said silicide layers, said first metallization layer being made of said metal material;

a second metallization layer that is in intimate contact with said first metallization layer, similar in geometry to said first metallization layer, and made of a material having a smaller resistivity than the material of said first metallization layer; and

conductive interconnects formed in the same layer as said gate electrode and connected with said first metallization layer via at least one contact.

6. A device according to claim 5, wherein said first metallization layer consists mainly of an element selected from the group consisting of titanium, molybdenum, tungsten, platinum, chromium, and cobalt.

7. A method of fabricating a semiconductor device,

comprising the steps of:

forming a gate insulator layer and a gate electrode on an active layer;

etching said gate insulator layer to form a gate insulator film wider than said gate electrode;

forming a first metallization layer out of a material in intimate contact with said active layer;

reacting said active layer with said first metallization layer to form silicide layers self-aligned to said gate insulator film; and

selectively etching said first metallization layer.

8. A method according to claim 7, wherein a step of forming a second metallization layer out of a material having a resistivity smaller than that of the material of said first metallization layer is performed between said step of reacting said active layer with said first metallization layer and said step of selectively etching said first metallization layer such that said second metallization layer is in intimate contact with said first metallization layer.

9. A method according to claim 7, wherein a step of forming an n- or p-type doped region in a self-aligned manner in the active region, using said gate electrode, is performed between said step of forming said gate insulator layer and said gate electrode on the active layer and said step of etching said gate insulator layer.

10. A method according to claim 9, wherein a step of forming a more heavily doped region than said n- or p-type doped region is performed between said step of etching said gate

insulator layer and said step of forming said first metallization layer such that said more heavily doped region is of the same conductivity type as said n- or p-type doped region.

11. A method according to claim 7, wherein a step of forming an n- or p-type doped region in said active region in a self-aligned manner, using said gate electrode or both said gate electrode and said gate insulator film, is performed between said step of etching said gate insulator layer and said step of forming said first metallization layer.

12. A method according to claim 7, wherein after said step of selectively etching said first metallization layer, an interlayer dielectric is deposited, said interlayer dielectric is etched to form contact holes reaching said first metallization layer, and a top layer of interconnect metal connected with said first metallization layer via said contact holes is formed.

add A1

add B1

add C1

add D3